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CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (currently amended). A method for transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit, the method which comprises:

associating the hardware arithmetic-logic unit with at least one table memory, the hardware arithmetic-logic unit obtaining data required during a computing operation from the table memory and/or the hardware arithmetic-logic unit storing data computed during a computing operation in the table memory; and reading and/or writing from the digital processor to the table memory by:

preselecting a base address in the table memory dependent on a data type of data to be transmitted; ~~and~~

computing a plurality of addresses according to a prescribed arithmetic computation rule in hardware by taking the preselected base address as a starting point resulting in a computed plurality of addresses; and

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accessing the table memory with the digital processor
~~using the computed taking the preselected base address as~~
~~a starting point for computing, according to a prescribed~~
~~arithmetic computation rule in hardware, a plurality of~~
addresses used for consecutive read access operations
and/or consecutive write access operations in the table
memory.

2 (original). The method according to claim 1, which further
comprises:

storing a plurality of base addresses associated with a
plurality of different data types in a base address register,
the base address that was preselected being one of the
plurality of base addresses; and

performing the step of preselecting the base address by using
the processor to set a selection bit associated with the base
address.

3 (original). The method according to claim 2, which further
comprises:

prescribing the plurality of base addresses unalterably in
hardware.

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4 (original). The method according to claim 1, which further comprises:

providing the arithmetic computation rule for computing the plurality of addresses in the table memory as an incrementation rule or a decrementation rule.

5 (original). The method according to claim 1, which further comprises:

programming the base address with the digital processor.

6 (original). The method according to claim 1, which further comprises:

with the digital processor, programming at least one information item selected from a group consisting of information relating to a number of data items being written to or read from a plurality of memory subareas associated with the base address, information about a block size of data blocks, information about a decoding rate, and information about utilized convolution polynomials.

7 (original). The method according to claim 1, which further comprises:

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providing a first data type of the plurality of data types as soft input values for channel decoding that are intended for a decoder hardware arithmetic-logic unit; and

with the digital processor, programming how many soft input values per unit time can be stored in a memory subarea associated with the first data type.

8 (original). The method according to claim 1, which further comprises:

providing a second data type as trace back values computed by a decoder hardware arithmetic-logic unit; and

with the digital processor, programming how many states the trace back values need to include.

9 (original). The method according to claim 1, which further comprises:

choosing a packing mode causing a plurality of data words, output by the processor for performing the step of accessing the table memory, to be combined to form a memory data word for the table memory.

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10 (original). The method according to claim 1, which further comprises:

choosing an unpacking mode causing a memory data word, read from the table memory when performing the step of accessing the table memory, to be broken down into a plurality of data words before being input into the processor.

11 (currently amended). A circuit configuration for transmitting data of a plurality of data types between a processor and a hardware arithmetic-logic unit, comprising:

said processor and said hardware arithmetic-logic unit;

at least one table memory associated with the hardware and arithmetic logic unit, said table memory for providing data to the hardware and arithmetic logic unit required for a computing operation of the hardware and arithmetic logic unit, said table memory for storing data computed in a computing operation of the hardware and arithmetic logic unit;

an input and/or output memory having a prescribed address used by said processor to access said input and/or output memory for data input/output;

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a base address memory device for storing, for each data type,
a base address for said table memory; and

a hardware address computation circuit for, taking the base
address as a starting point, applying an arithmetic
computation rule to produce a plurality of addresses enabling
used by the digital processor to consecutively accesses said
table memory.

12 (original). The circuit configuration according to claim
11, wherein:

said base address memory device is an external base address
register designed such that in order to select the base
address, said processor sets a selection bit associated with
the base address.

13 (original). The circuit configuration according to claim
11, wherein said base address memory device is a read only
memory.

14 (original). The circuit configuration according to claim
11, wherein said base address memory device is a rewritable
memory that can be programmed by the digital processor.

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15 (original). The circuit configuration according to claim 11, further comprising:

a configuration memory;

said table memory including memory subareas; and

said configuration memory for storing information selected from a group consisting of information relating to a number of data items being written to or read from a plurality of said memory subareas associated with the base address, information about a block size of data blocks, information about a decoding rate, and information about utilized convolution polynomials.

16 (original). The circuit configuration according to claim 11, further comprising:

a multiplexer and buffer device for assembling a plurality of data words output by said processor to form a memory data word intended for being stored at an address in said table memory.

17 (original). The circuit configuration according to claim 11, further comprising:

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a demultiplexer and buffer device for, before being input into said processor, breaking down a memory data word read from said table memory into a plurality of data words.

18 (original). The circuit configuration according to claim 11, wherein said table memory has a prescribed memory word length.

19 (original). The circuit configuration according to claim 11, wherein:

said hardware arithmetic-logic unit is a Viterbi hardware arithmetic-logic unit.

20 (original). The circuit configuration according to claim 11, wherein:

said hardware arithmetic-logic unit includes an equalizer hardware arithmetic-logic unit and a decoder hardware arithmetic-logic unit;

said processor includes a data transmission connection to said equalizer hardware arithmetic-logic unit; and

said processor includes a data transmission connection to said decoder hardware arithmetic-logic unit.